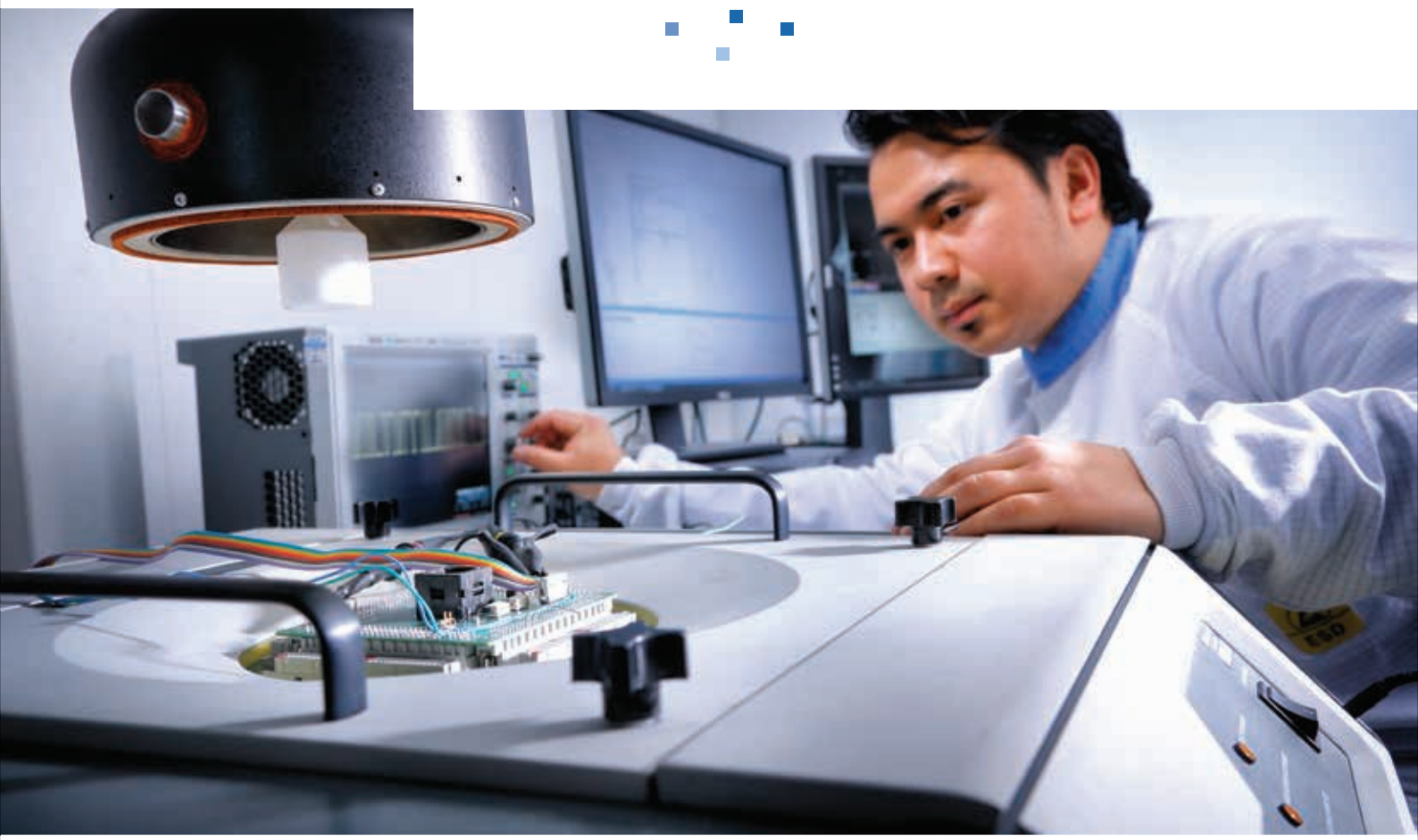
MASER
ENGINEERING



ESD AND LATCH-UP TEST SERVICES

- ELECTRO STATIC DISCHARGE TESTING
- COMPONENTS AND SYSTEMS
- HBM – MM – CDM – ETGL MODELS
- ESDA – JEDEC – MIL – AEC – IEC STANDARDS
- LATCH-UP TESTING WITH DYNAMIC SETUP
- VF-TLP ESD PROTECTION EVALUATION

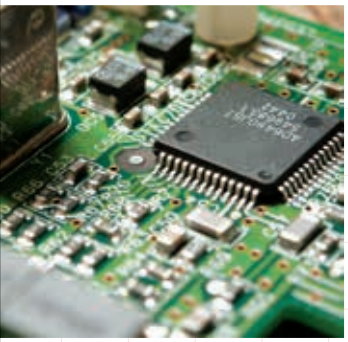
ESD AND LATCH-UP TEST SERVICES

ESD TESTING OF ELECTRONIC COMPONENTS

- ESD protection circuitry test of IC's and small modules
- HBM and MM testing up to 8kV on Mk.2 systems
- CDM testing up to 2kV on RCDM-3 systems
- Test according JEDEC-ESDA-Q100-MIL-IEC standards
- HBM and CDM ESD tests under ISO-17025 accreditation
- Scimitar™ software for test control and data processing

ESD TESTING OF ELECTRONIC SYSTEMS

- ESD protection circuitry test of electronic systems
- Contact and Field discharge up to 30kV with NSG-438
- ISO 10605 automotive range of discharge networks
- IEC 61000-4-2 networks including 330Ω/150pF
- Test according IEC 61000-4-2 & ISO 10605 standards
- Dedicated system setup and GND plates



LATCH-UP TESTING OF INTEGRATED CIRCUITS

- Latch-Up phenomena sensitivity test of IC's
- LU testing with up to 5 V/I power supply domains
- 64k per pin vector memory and 512 pins on our Mk.2 systems
- Test according JEDEC-47 and Q100 standards up to +175°C
- Latch-Up tests under ISO-17025 accreditation
- Scimitar™ software for test control and data processing

ESD PROTECTION CIRCUIT CHARACTERIZATION OF IC'S

- ESD protection circuit characterization of IC's
- VF-TLP up to 40A on IC and wafers up to 200 mm
- 2-port measurement
- 40GS/s pulse sampling
- 50 Ω system, 0.1-50ns pulse rise time, 1-100ns pulse width
- Engineering cooperation with FhG EMFT on VF-TLP and M-CDM

MASER Engineering is an ESDA standardization committee member.

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